

CLAIMS

1. A digital data processing device, comprising:
 - a memory, said memory containing a segment table, said segment table having a plurality of segment table entries corresponding to respective segments in a first address space, each segment table entry containing pre-fetch data identifying a plurality of sub-units of the corresponding segment as pre-fetch candidates;
 - at least one processor;
 - at least one structure for temporarily storing data from said memory in a location more accessible to said processor; and
 - a pre-fetch engine, said pre-fetch engine performing at least one pre-fetch action, said at least one pre-fetch action comprising pre-fetching selective data with respect to a sub-unit of said plurality of sub-units of a segment from said memory into said at least one structure for temporarily storing data, said pre-fetch engine selecting said selective data for pre-fetching using said pre-fetch data in said segment table.
2. The digital data processing device of claim 1, wherein said pre-fetch action comprises pre-fetching address translation data with respect to said sub-unit into at least one address translation cache structure.
3. The digital data processing device of claim 2, wherein said at least one address translation cache structure comprises a translation look-aside buffer.
4. The digital data processing device of claim 2, wherein said at least one address translation cache structure comprises an effective-to-real address translation table (ERAT).
5. The digital data processing device of claim 1, wherein said digital data processing device automatically generates said pre-fetch data.

1 6. The digital data processing device of claim 5, wherein said pre-fetch data comprises
2 a plurality of up-or-down counters corresponding to respective sub-units of the
3 corresponding segment, each up-or-down counter being incremented on the occurrence of
4 at least one pre-defined event of a first set with respect to the corresponding sub-unit and
5 being decremented on the occurrence of at least one pre-defined event of a second set with
6 respect to the corresponding sub-unit.

1 7. The digital data processing device of claim 6,
2 wherein each said up-or-down counter is incremented if data with respect to the
3 corresponding sub-unit is loaded into a first structure for temporarily storing data, and a data
4 reference is made to said corresponding sub-unit while the data is in said first structure for
5 temporarily storing data; and
6 wherein each said up-or-down counter is decremented if data with respect to the
7 corresponding sub-unit is loaded into said first structure for temporarily storing data, and no
8 data reference is made to said corresponding sub-unit while the data is in said first structure
9 for temporarily storing data.

1 8. The digital data processing device of claim 1, wherein said sub-unit is a page of
2 memory.

1 9. The digital data processing device of claim 1, wherein said segment table translates
2 segment identifiers in an effective address space of an executing task to segment identifiers
3 in a global virtual address space, and wherein a page table translates segment identifiers in
4 the global virtual address space to pages in said memory.

1 10. The digital data processing device of claim 1, wherein said pre-fetch action is
2 performed responsive to an occurrence of an event of a first type.

1 11. The digital data processing device of claim 10, wherein said event of said first type

comprises generating a reference to data within the corresponding segment.

12. A processor for a digital data processing device, comprising:

an instruction unit determining instruction sequences;

an execution unit execution instructions in said instruction sequences;

at least one cache for temporarily storing data from a memory of said digital data processing device for use by at least one of said instruction unit and said execution unit;

a pre-fetch engine, said pre-fetch engine performing at least one pre-fetch action, said at least one pre-fetch action comprising pre-fetching selective data with respect to a sub-unit of said plurality of sub-units of a segment from said memory into said at least one structure for temporarily storing data, said pre-fetch engine selecting said selective data for pre-fetching using pre-fetch data associated with respective segments in said memory, said pre-fetch data identifying a plurality of sub-units of a corresponding segment as pre-fetch candidates.

13. The processor for a digital data processing device of claim 12, wherein said pre-fetch action comprises pre-fetching address translation data with respect to said sub-unit into at least one address translation cache structure.

14. The processor for a digital data processing device of claim 12, wherein said pre-fetch data comprises a plurality of automatically maintainable up-or-down counters corresponding to respective sub-units of the corresponding segment, each up-or-down counter being incremented on the occurrence of at least one pre-defined event of a first set with respect to the corresponding sub-unit and being decremented on the occurrence of at least one pre-defined event of a second set with respect to the corresponding sub-unit.

15. The processor for a digital data processing device of claim 14, wherein each said up-or-down counter is incremented if data with respect to the corresponding sub-unit is loaded into a first structure for temporarily storing data, and a data

1 reference is made to said corresponding sub-unit while the data is in said first structure for
2 temporarily storing data; and

3 wherein each said up-or-down counter is decremented if data with respect to the
4 corresponding sub-unit is loaded into said first structure for temporarily storing data, and no
5 data reference is made to said corresponding sub-unit while the data is in said first structure
6 for temporarily storing data.

1 16. The processor for a digital data processing device of claim 12, wherein said sub-unit
2 is a page of memory.

1 17. The processor for a digital data processing device of claim 12, wherein said pre-fetch
2 action is performed responsive to an occurrence of an event of a first type.

1 18. The processor for a digital data processing device of claim 17, wherein said event of
2 said first type comprises generating a reference to data within the corresponding segment.

1 19. A method for pre-fetching data within a digital data processing device, comprising:
2 associating with each of a plurality of segments of a first address space of said digital
3 data processing device, a respective plurality of sub-units of the corresponding segment;
4 determining that a processor has generated a reference to an address within a first
5 segment of said plurality of segments; and
6 responsive to said determining step, initiating at least one pre-fetch action with
7 respect to said first segment, said at least one pre-fetch action comprising pre-fetching
8 selective data with respect to each sub-unit of the plurality of sub-units associated with said
9 first segment by said associating step.

20. The method for pre-fetching data of claim 19, wherein said pre-fetch action comprises pre-fetching address translation data with respect to each said sub-unit of the plurality of sub-units associated with said first segment into at least one address translation cache structure.

21. The method for pre-fetching data of claim 20, wherein said pre-fetch action further comprises pre-fetching at least some data within each of a plurality of said sub-units associated with said first segment responsive to pre-fetching said address translation data.